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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,057	10/09/2003	John W. Rapp	1934-14-3	3242

7590 08/07/2007

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EXAMINER	
FRANKLIN, RICHARD B	

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
08/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/684,057	RAPP ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24,26-29,32-36 and 38-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-10,12-24,26-29,32-36 and 38-40* is/are rejected.

7)☒ Claim(s) *2,6 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/8/06,2/16/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 24, 26 – 29, 32 – 36, and 38 – 40 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 May 2007 has been entered.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on 08 November 2006 and 16 February 2007 have been considered by the examiner. However, the IDS filed 08 November 2006 lists US 2004/181621 A1, which is not a valid number of a US Patent Application Publication. Therefore, the reference has not been considered. However, the Examiner notes that US 2004/0181621 A1 is a valid US Patent Application Publication to the Applicant listed on the IDS. It appears applicant incorrectly left out the "0" after the "2004/" in the reference number. The Examiner respectfully asks Applicant to double check the reference number and submit another IDS listing the correct reference.

Response to Arguments

4. Applicant's arguments filed 21 May 2007 have been fully considered but they are not persuasive.

Applicant argues that the relied upon reference, US Patent No. 6,308,311 (hereinafter Carmichael), does not teach that the programmable logic integrated circuit is operable to function as an endpoint on an industry standard bus as required by independent claim 1. Applicant argues that the programmable logic integrated circuit of Carmichael cannot be an endpoint of an industry standard bus because it is an interface between the host system and the target FPGA (See Remarks Filed 21 May 2007; Page 15 Lines 1 – 8). However, the Examiner submits that the programmable logic integrated circuit of Carmichael is functioning as an endpoint of the industry standard bus. The industry standard bus (Carmichael; Figure 3 Items 33 and 35) ends at the FPGA 32. The bus 48 between the interface and the target FPGA 10 is a different set of signal lines (Carmichael; Col 5 Lines 38 – 39), and not the same bus as bus 33 and 35. Therefore, the FPGA 32 of Carmichael is the endpoint of the industry standard bus 33 and 35.

In response to the Examiners description of the definition of an "industry standard bus," applicant has argued that such a bus includes a bus structure and a corresponding communications protocol that the devices connected to the bus must use in order to communicate over the bus (See Remarks Filed 21 May 2007; Page 15 Lines 15 – 26). However, the Examiner contends that a wire still meets this definition of an

"industry standard bus." Any communications between two computer systems must follow a certain protocol. That way, the receiving computer system will understand what the transmitting computer system has sent. If no predetermined protocol is used and each device transmits and understands information in its own way, no computer systems would be able to communicate with each other. A single wire can be used for communicating data between computer systems and therefore, such communications must follow a predetermined protocol in order for the communication to take place. Therefore, a single wire still meets the definition of an "industry standard bus."

As per claim 13, Applicant argues that the combination of Carmichael and US Patent Application Publication No. 2003/0177223 (hereinafter Erickson) does not disclose the claimed invention. Applicant proposes the question of "why would the multiple FPGAs need to be interconnected since they are running in parallel executing respective firmware versions?" (See Remarks filed 21 May 2007; Page 16 Line 27 – Page 17 Line 9). It is not clear to the Examiner what the Applicant is arguing here. Erickson clearly shows the multiple FPGAs are interconnected (Erickson; Figure 1 Connection between Items 112 and 114).

As per claims 16, 20, and 24, Applicant argues that Carmichael does not teach a direct connection between the FPGA 32 and the industry standard bus (See Remarks filed 21 May 2007; Page 17 Lines 10 – 17). However, in view of the interpretation of the industry standard bus set forth above, busses 33 and 35 of Figure 3 are considered to

be industry standard busses. Therefore, Carmichael does teach a direct connection between the industry standard bus and the FPGA.

As per claims 32 and 36, Applicant argues that Carmichael does not teach directly downloading firmware codes into the programmable logic integrated circuit. Applicant notes that Carmichael uses a microcontroller between the USB and serial busses to communicate with the FPGA (See Remarks filed 21 May 2007; Page 17 Lines 18 – 29). However, the Examiner did not state in the rejection that the direct downloading was through the microcontroller 34. The rejection states that firmware codes are downloaded directly into the FPGA 32 from the SPROM memory 38 through a serial port 32s. The direct downloading relied upon in the rejection has nothing to do with the microcontroller 34. The serial bus between the SPROM 38 and the FPGA 32 meets the industry standard bus limitation of the claims. Therefore, the rejection of claim 32 is proper and remains.

Claim Objections

5. Claims 12 and 20 are objected to because of the following informalities:

- Claim 12 lists "Currently Amended" as its current status. However, claim 12 does not show any changes using underlining or strikethrough, and the Examiner is not able to find any differences between the current claim and the claim presented in the previous response. Therefore, it is believed by the Examiner that the current status of the claim is "Previously Presented."

- Claim 20 lists "Previously Presented" as its current status. However, claim 20 clearly shows additions to the claim at the underlines sections on line 8 and deletions at the strikethrough section on line 9. Therefore, it is believed by the Examiner that the current status of the claim is "Currently Amended."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 13 – 15 and 39 – 40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "the industry standard bus" in line 6 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claims 14 – 15 are rejected for inheriting the deficiencies of base claim 13 as shown above.

Claim 39 recites the limitation "the Rapid I/O bus protocol" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

The Examiner has interpreted the limitation as reciting "a Rapid I/O bus protocol."

As per claim 39, the use of the trademark RAPID I/O™ as a limitation of the claim to identify or describe a particular product renders the claim indefinite. The claim scope is uncertain since the trademark cannot be used properly to identify any particular material or product. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). See also MPEP § 2173.05(u).

Claim 40 is rejected for inheriting the deficiencies of base claim 39 as shown above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4 – 5, 7, 9 – 10, 12, 16, 20, 23, 32 – 33 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,308,311 (hereinafter Carmichael).

As per claim 1, Carmichael teaches a programmable logic integrated circuit (Figure 3 Item 32) operable to function as an endpoint of an industry standard bus (Figure 3 Items 33 and 35, See "Response to Arguments" above), an interface ([Connection between Item 32 and Items 33 and 35]) to the industry standard bus being operable through the interface to receive multiple versions of firmware from an external source (Col 6 Lines 22 – 35, Col 7 Lines 40 – 65), each version of firmware

representing a corresponding operating configuration; store the multiple versions of firmware in a memory (Figure 3 Item 36, Col 7 Lines 45 – 53); download a selected one of the versions of firmware from the memory (Col 6 Lines 11 – 18, Col 7 Lines 58 – 60); and configure itself using the downloaded firmware to operate in the corresponding operating configuration (Col 7 Lines 58 – 63).

As per claim 4, Carmichael also teaches wherein the memory comprises memory external to the programmable logic integrated circuit (Fig 3 Items 36 or 38).

As per claim 5, Carmichael teaches a programmable logic integrated circuit (Figure 3 Item 32) operable to function as an end point on an industry standard bus (Figure 3 Items 33 and 35, See "Response to Arguments" above), an interface ([Connection between Items 32 and Items 33 and 35]) to the industry standard bus, and being operable to, download from a memory storing a plurality of versions of firmware (Figure 7a Item 36) a first firmware that represents a first configuration (Col 6 Lines.22 – 35); configure itself using the first firmware configuration (Col 6 Lines 27 – 31); operate in the first configuration (Col 6 Lines 31 – 35); download from the memory a second firmware that represents a second configuration (Col 7 Lines 58 – 60); configure itself using the second firmware version (Col 7 Lines 58 – 60); and operate in the second configuration (Col 7 Lines 40 – 65).

As per claim 7, Carmichael teaches a programmable circuit unit (Figure 3 Item 30) comprising a memory (Figure 3 Item 36), a programmable logic integrated circuit (Figure 3 Item 32) coupled to the memory, the programmable logic integrated circuit operable to function as an endpoint on an industry standard bus (Figure 3 Items 33 and 35, See "Response to Arguments" above), the programmable circuit including an industry standard bus interface ([Connection between Items 32 and Items 33 and 35]), the programmable logic integrated circuit being operable through the industry standard bus interface to, receive multiple versions of firmware that represents corresponding operating configurations of the programmable circuit from an external source (Col 6 Lines 22 – 35, Col 7 Lines 40 – 65), store the firmware in a memory (Figure 3, Col 7 Lines 49 – 53), and download the firmware from the memory (Col 7 Lines 58 – 60), and configure itself using the downloaded firmware to operate in the corresponding operating configuration (Col 7 Lines 58 – 63).

As per claim 9, Carmichael also teaches that the programmable circuit comprises a field-programmable gate array (FPGA) (Figure 3 Item 32).

As per claim 10, Carmichael teaches a programmable circuit unit (Figure 3 Item 30) comprising a pipeline bus (Figure 3 Items 33 and 35) operable to communicate data through an industry standard bus protocol (See "Response to Arguments" above); a memory operable to store a plurality of versions of firmware, each version respectively representing a corresponding configurations (Figure 3 Items 36 and 38); a

programmable logic integrated circuit (Figure 3 Item 32) coupled to the memory and operable to function as an endpoint on the pipeline bus (See "Response to Arguments" above), the programmable logic integrated circuit including an interface to the pipeline bus ([Connection between Item 32 and Items 33 and 35]) and being operable to download from the memory a first selected one of the versions of firmware (Col 6 Lines 27 – 35), operate in the first configuration (Col 6 Lines 31 – 35), download from the memory a second selected one of the versions of firmware (Col 7 Lines 58 – 60), and operate in the second configuration (Col 7 Lines 40 – 65).

As per claim 12, Carmichael also teaches that the programmable circuit unit can load the second firmware while operating in the first configuration (Col 7 Lines 58 – 60).

As per claim 16, Carmichael teaches a computing machine (Figure 3 Item 30) comprising a processor (Figure 3 Item 34); an industry standard bus (Figure 3 Item 33 and 35) coupled to the processor, the industry standard bus adapted to be coupled to standard peripheral devices; a memory that stores a plurality of firmware configurations (Figure 3 Items 36 and 38); and a programmable logic integrated circuit (Figure 3 Item 32) coupled to the memory, and the programmable logic integrated circuit directly coupled to the industry standard bus and through this bus to the processor ([Connection between Items 32 and 34 is directly through Items 33 and 35]), the programmable logic integrated circuit operable to receive from the processor a new firmware configuration that represents a new configuration of the programmable circuit (Col 7 Lines 40 – 44),

store the new firmware configuration in the memory (Col 7 Lines 49 – 53), and download the new firmware configuration from the memory in response to the processor (Col 7 Lines 58 – 60).

As per claim 20, Carmichael teaches a computing machine (Figure 3) that includes a processor (Figure 3 Item 34); an industry standard bus coupled to the processor (Figure 3 Items 33 and 35, See "Response to Arguments" above), the industry standard bus adapted to be coupled to standard peripheral devices; a memory (Figure 3 Items 36 and 38) to store a plurality of versions of firmware, each version respectively represent configurations of a programmable logic integrated circuit (Figure 3. Item 32), the programmable logic integrated circuit being coupled to the memory and being coupled directly to the industry standard bus and through this bus to the processor ([Connection between Items 32 and 34 is directly through Items 33 and 35]), the programmable logic integrated circuit operable to download a selected one of the firmware versions from the memory (Col 6 Lines 27 – 35), operate in the configuration corresponding to the downloaded firmware version, download a different firmware version from the memory in response to the processor (Col 7 Lines 49 – 60), and operate in the configuration corresponding to the different firmware version (Col 7 Lines 40 – 65).

As per claim 23, Carmichael also teaches that the computing machine processor can send the selected firmware to the programmable logic integrated circuit (Col 7 Lines

49 – 53), and that the programmable-circuit can load the different firmware into the memory in response to the processor while operating in the configuration corresponding to the selected one of the firmware versions (Col 7 Lines 49 – 53).

As per claim 32, Carmichael teaches a method comprising storing in a memory (Figure 3 Items 36 or 38) a plurality of firmware codes (Figure 7a Item 36), each firmware code representing a configuration of a programmable logic integrated circuit (Col 6 Lines 22 – 35); downloading over an industry standard bus (Figure 3 [bus between items 38 and 32a], See "Response to Arguments" above) directly into the programmable logic integrated circuit a first firmware code that represents a first configuration (Col 6 Lines 22 – 27); operating the programmable logic integrated circuit in the first configuration (Col 6 Lines 27 – 35); downloading into the programmable logic integrated circuit second firmware that represents a second configuration (Col 7 Lines 40 – 44); and operating the programmable logic integrated circuit in the second configuration after downloading the second firmware (Col 7 Lines 40 – 65).

As per claim 33, Carmichael also teaches sending the second firmware to the programmable logic integrated circuit (Col 7 Lines 49 – 53), loading the second firmware into a memory with the programmable logic integrated circuit while the programmable logic integrated circuit is operating in the first configuration (Col 7 Lines 49 – 53), and downloading the second firmware from the memory into the programmable logic integrated circuit (Col 7 Lines 58 – 60).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent Application Publication No. 2003/0061409 (hereinafter RuDusky).

As per claim 3, Carmichael teaches the programmable circuit with memory as described per claim 1 (See rejection of claim 1 above).

Carmichael does not teach that the memory is a non-volatile memory.

However, RuDusky teaches a programmable circuit that uses a non-volatile electrically erasable and programmable read-only memory (EEPROM) to store configuration information (RuDusky; Paragraph [0049]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Carmichael to include a non-volatile memory to store configuration information because doing so would allow for the configuration information to remain in the memory even with no power to the system.

As per claim 8, Carmichael teaches the programmable circuit with memory as described per claim 7 (See rejection of claim 7 above).

Carmichael does not teach that the memory is an EEPROM.

However, RuDusky teaches a programmable circuit that uses an EEPROM to store configuration information (RuDusky; Paragraph [0049]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of to include an EEPROM to store configuration information because doing so would allow for the configuration information to remain in the memory even with no power to the system.

9. Claims 13 – 15, 17 – 18, 24, 27 – 29, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent Application Publication No. 2003/0177223 (hereinafter Erickson).

As per claim 13, Carmichael teaches a programmable-circuit unit (Carmichael; Figure 3 Item 30) comprising a memory to hold different firmware configurations (Carmichael; Figure 3 Items 36 and 38); and a first programmable logic integrated circuit (Carmichael; Figure 3 Item 32) coupled to the memory and including an industry standard interface (Carmichael; Connection between Item 32 and Items 33 and 35, See "Response to Arguments" above), the first programmable logic integrated circuit operable to receive the firmware configurations via the industry standard bus (Carmichael; Figure 3 Items 33 and 35) and to store these configurations in the memory (Carmichael; Col 7 Lines 40 – 53), and wherein the first programmable logic integrated

circuit is further operable to, download a first selected one of the firmware configurations from the memory (Carmichael; Col 6 Lines 27 – 35), operate in the configuration corresponding to the first selected firmware configuration (Carmichael; Col 6 Lines 31 – 35), download a first different one of the firmware configurations from the memory (Carmichael; Col 7 Lines 58 – 60), and operate in the configuration corresponding to the first different firmware configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable circuit coupled to the memory and first programmable circuit that is operable to download a second selected firmware from the memory, operate in the second selected configuration, download a second different firmware from the memory, and operate in the second different configuration.

However, Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or field programmable gate arrays (FPGAs) (Erickson; Paragraph [0013] Lines 14 – 19) running different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include multiple FPGAs that run different versions of firmware that is updated because doing so allows firmware to be changed in a system with higher computing power than a single FPGA system.

As per claim 14, Carmichael also teaches receiving the first and second configuration from an external source via the industry standard bus while operating in the first configuration and storing the first and second configuration in the memory while operating in the first configuration (Carmichael; Col 7 Lines 49 – 53).

As per claim 15, Carmichael also teaches that the programmable logic integrated circuit is a FPGA (Carmichael; Figure 3 Item 32).

As per claim 17, Carmichael teaches the computing machine with a processor coupled to a programmable logic integrated circuit unit as described per claim 16 (See rejection of claim 16 above).

Carmichael does not teach determining whether the firmware is already stored in the memory before sending the firmware to the programmable circuit, and sending the firmware to the programmable circuit only if the firmware is not already stored in the memory.

However, Erickson teaches determining if a firmware is stored in a memory coupled to the programmable circuit (Erickson; Figure 3 Items 320 – 360) and only sending the firmware to the programmable circuit if the second firmware is not stored in the memory (Erickson; Figure 3 Item 360).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the checking to see if the firmware is already stored in the memory and not sending the

firmware if it is already stored because doing so reduces the chance of sending data that has already been sent and thereby wasting processing power on a data transfer that is not needed.

As per claim 18, Erickson also teaches a configuration registry (Erickson; Figure 1 Items 130 and 140) that stores firmware (Erickson; Figure 1 Item 132, Paragraph [0014]) and indicates that the firmware represents a desired configuration (Erickson; Paragraph [0015]), and that the processor is operable to download the firmware from the configuration registry into the programmable circuit (Erickson; Paragraph [0017] Lines 9 – 13).

As per claim 24, Carmichael teaches a computing machine comprising a processor (Carmichael; Figure 3 Item 34); an industry-standard bus (Carmichael; Figure 3 Items 33 and 35) coupled to the processor and adapted to be coupled to standard peripheral devices; a memory to hold different firmware configurations (Carmichael; Figure 3 Items 36 and 38); a first programmable logic integrated circuit (Carmichael; Figure 3 Item 32) coupled to the memory and coupled directly to the industry standard bus and through this bus to the processor, the first programmable logic integrated circuit operable to download a first configuration from the memory (Carmichael; Col 6 Lines 27 – 35), operate in the first configuration, download a second configuration from the memory in response to the processor (Carmichael; Col 7 Lines 58 – 60), and operate in the second configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable logic integrated circuit coupled to the memory and the first programmable circuit, and coupled through the first programmable logic integrated circuit to the industry standard bus and through this bus to the processor, the second programmable logic integrated circuit operable to download a third firmware from the memory, operate in the third configuration, download a fourth firmware from the memory in response to the processor, and operate in the fourth configuration.

However, Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or FPGAs (Erickson; Paragraph [0013] Lines 14 – 19) running different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include multiple FPGAs that run different versions of firmware that is updated because doing so allows firmware to be changed in a system with higher computing power than a single FPGA system.

As per claim 27, Carmichael also teaches receiving the second configuration from an external source and storing it in memory while operating in the first configuration (Carmichael; Col 7 Lines 49 – 53).

As per claim 28, Erickson also teaches a separate memory unit to hold firmware information for each processor (Erickson; Figure 1 Items 120 and 122).

As per claim 29, Carmichael in combination with Erickson obviously teaches that the separate memories are disposed on separate integrated circuits because putting memories on different integrated circuits would be an obvious engineering choice.

Such a modification is considered to be within the level of ordinary skill in the art as set forth by the following legal precedents; See Making Integral – *In re Larson*, 340 F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965); *In re Wolfe*, 251 F.2d 854, 855, 116 USPQ 443, 444 (CCPA 1958).

As per claim 34, Carmichael teaches the method as described per claim 32 (See rejection of claim 32 above) and loading the second firmware into the memory with the programmable logic integrated circuit while operating in the first configuration (Carmichael; Col 7 Lines 58 – 60) and downloading the second firmware from the memory into the programmable logic integrated circuit (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach determining if the second firmware is stored in a memory coupled to the programmable logic integrated circuit and sending the second firmware to the programmable logic integrated circuit only if the second firmware is not stored in the memory.

However, Erickson teaches determining if the second firmware is stored in a memory coupled to the programmable logic integrated circuit (Erickson; Figure 3 Items 320 – 360) and only sending the second firmware to the programmable logic integrated circuit if the second firmware is not stored in the memory (Erickson; Figure 3 Item 360).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the checking to see if the firmware is already stored in the memory and not sending the firmware if it is already stored because doing so reduces the chance of sending data that has already been sent and thereby and wasting processing power on a data transfer that is not needed.

As per claim 36, Carmichael teaches a first programmable logic integrated circuit (Carmichael; Figure 3 Item 32) coupled to a memory that stores a plurality of firmware codes (Carmichael; Figure 3 Items 36 and 38) and operable to directly download a first configuration (Carmichael; Col 6 Lines 27 – 35) over an industry-standard bus (Carmichael; Figure 3 [bus between items 38 and 32a], See "Response to Arguments" above), operate in the first configuration, directly download a third configuration from the memory (Carmichael; Col 7 Lines 58 – 60), and operate in the third configuration (Carmichael; Col 7 Lines 40 – 65).

Carmichael does not teach a second programmable logic integrated circuit coupled to the memory and the first programmable logic integrated circuit that is operable to directly download a second firmware from the memory, operate in the

second configuration, directly download a fourth firmware from the memory, and operate in the fourth configuration.

However, Erickson teaches a system that has multiple processors (Erickson; Figure 1 Items 112 and 114) or FPGAs (Erickson; Paragraph [0013] Lines 14 – 19) running different versions of firmware (Erickson; Figure 1 Items 116 and 118). The firmware running on the processors is also updated (Erickson; Paragraph [0017] Lines 9 – 13).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include multiple FPGAs that run different versions of firmware that is updated because doing so allows for firmware to be changed in a system with higher computing power than a single FPGA system.

10. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent No. 6,096,091 (hereinafter Hartmann).

As per claim 19, Carmichael teaches the computing machine with a processor coupled to a programmable logic integrated circuit unit as described per claim 16 (See rejection of claim 16 above).

Carmichael does not teach that the programmable logic integrated circuit programmable circuit includes a hardwired pipeline that can operate on data.

However, Hartmann teaches the use of a reconfigurable programmable circuit unit that includes a pipeline unit (Hartmann; Figure 2, Col 2 Lines 32 – 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include a pipeline unit because doing so would speed up data processing of the system.

11. Claims 21 – 22, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent No. 6,893 873 (hereinafter Moore).

As per claim 21, Carmichael teaches the computing machine as described per claim 20 (See rejection of claim 20 above).

Carmichael does not teach that the processor has a first test port, the programmable logic integrated circuit has a second test port coupled to the first test port, and the processor is able to load the selected one of the firmware into memory via the first and second test ports.

However, Moore teaches a programmable circuit with a test port (Moore; Figures 2A – 2C Item 206). The programmable circuit performs a self-test (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and can send the result to a processor through the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the test ports and data transfer through the test ports because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

As per claim 22, Moore also teaches that the processor comprises a first test port, the programmable logic integrated circuit comprises a second test port that is coupled to the first test port (Moore; Figures 2A – 2C Item 206), the programmable logic integrated circuit can perform a self-test and send self-test data to the processor via the first and second test ports (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31), and firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

As per claim 35, Carmichael teaches the method as described per claim 32 (See rejection of claim 32 above).

Carmichael does not teach that operating the programmable logic integrated circuit in the first configuration comprises testing the programmable logic integrated circuit, and downloading the second firmware comprises downloading the second firmware only if the programmable logic integrated circuit passes testing.

However, Moore teaches a programmable logic integrated circuit with a test port (Moore; Figures 2A- 2C Item 206). The programmable logic integrated circuit performs a self-test (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31) and can send the result to a

processor through the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67). Firmware is then loaded into a memory through the test ports if the self-test results are appropriate (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael to include the test ports, self-test, and data transfer through the test ports only if a certain test result was discovered because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

12. Claims 26 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent Application Publication No. 2003/0177223 (hereinafter Erickson) and further in view of US Patent No. 6,893,873 (hereinafter Moore).

As per claim 26, Carmichael in combination with Erickson teaches a computing machine with multiple programmable circuits as described per claim 24 (See rejection of claim 24 above).

Carmichael in combination with Erickson does not teach the first and second programmable circuits to perform self-tests and provide the self-test data to the processor via the test ports, and then each programmable circuit loads a different firmware if the self-test data indicate a predetermined result of the self-tests.

However, Moore teaches the first and second programmable circuits to perform self-tests (Moore; Figure 3 Item 308, Col 5 Lines 28- 31) and provide the self-test data

to the processor via the test ports (Moore; Figure 2B, Col 5 Lines 57 – 67), and then each programmable circuit loads a different firmware if the self-test data indicate a predetermined result of the self-tests (Moore; Figure 2C, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael in combination with Erickson to include the test ports, self-test, and data transfer through the test ports only if a certain test result was discovered because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

As per claim 38, Carmichael in combination with Erickson teaches a method including multiple programmable circuits as described per claim 36 (See rejection of claim 36 above).

Carmichael in combination with Erickson does not teach testing the first and second programmable circuits, and wherein loading the firmware into the programmable circuits comprises loading the firmware only if the testing indicates that the programmable circuit is functioning as desired.

However, Moore teaches testing the first and second programmable circuits (Moore; Figure 3 Item 308, Col 5 Lines 28 – 31), and wherein loading the firmware into the programmable circuits comprises loading the firmware only if the testing indicates that the programmable circuit is functioning as desired (Moore; Figure 2c, Col 6 Lines 4 – 13).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Carmichael in combination with Erickson to include the loading of firmware though test ports because doing so eases the burden on a tester machine (Moore; Col 5 Lines 43 – 45).

13. Claims 39 – 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,308,311 (hereinafter Carmichael) in view of US Patent Application Publication No. 2006/0236018 (hereinafter Dao).

As per claim 39, Carmichael teaches the programmable circuit unit as described per claim 10 (see rejection of claim 10 above).

Carmichael does not teach wherein the industry standard bus protocol is the RAPID I/O™ bus protocol.

However, Dao teaches using the RAPID I/O™ bus protocol as a communication protocol (Dao; Paragraph [0192] Lines 5 – 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention as made to have modified the teachings of Carmichael to include the RAPID I/O™ bus protocol because doing so allows for the use of a high performance bus protocol (Dao; Paragraph [0192] Lines 5 – 8).

As per claim 40, Carmichael also teaches wherein the programmable circuit unit further comprises a router coupled to the pipeline bus (Carmichael; Figure 3 Item 34, Col 7 Lines 49 – 53)

Allowable Subject Matter

14. Claims 2, 6, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form ***including all of the limitations of the base claim and any intervening claims***.

15. The following is a statement of reasons for the indication of allowable subject matter:

Claim 2 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claim because the prior art of record fails to teach or suggest alone or in combination ***wherein the programmable logic integrated circuit comprises at least one hardwired pipeline, each hardwired pipeline operable to process respective data without executing program instructions; a communication shell coupled to the hardwired pipelines and operable to transfer data to and from the hardwired pipelines; and a communication interface coupled to the interface to the industry standard bus, the communication interface operable to communicate with the interface to the industry standard bus to transfer data to and from the programmable logic integrated circuit over the industry standard bus, and the communication interface further operable to transfer data to and from each hardwired pipeline via the communication shell***, as required by dependent claim 2, ***in combination with the other recited claim limitations*** (emphasis added). Support for the limitation can be found in the originally filed specification at Figure 4. Carmichael teaches a

programmable logic integrated circuit that is capable of receiving different firmware configurations and reconfiguring itself according to the new firmware. Carmichael also teaches storing the firmware configurations in a memory. However, Carmichael does not teach a hardwired pipeline that can process data without executing program instructions, and the communication shell or communication interface as described above. Neither RuDusky, Erickson, Hartman, Moore, nor Dao teach or suggest the structure described above either.

Claims 6 and 11 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claim because the prior art of record fails to teach or suggest alone or in combination a programmable logic integrated circuit ***wherein the second firmware version may only be received when operating in the first configuration***, as required by dependent claims 6 and 11, ***in combination with the other recited claim limitations*** (emphasis added). Support for this limitation can be found in the originally filed specification at Page 23 Lines 1 – 3. Carmichael teaches wherein the second firmware version may be received when operating in the first configuration, but does not state that this is the ***only*** time the second firmware can be received. Neither RuDusky, Erickson, Hartman, Moore, nor Dao teach or suggest the structure described above either.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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